CLAIMS

1. A method of fetching data from a memory component, said method comprising:

obtaining parameters relating to data fetching from said memory component based on an operating frequency of a bus; and

fetching said data from said memory component based on said obtained parameters.

2. The method of claim 1, wherein said parameters relate to a data transfer size.

3. The method of claim 2, wherein said parameters further relate to a threshold value.

4. The method of claim 1, wherein said parameters are obtained from values stored in a register corresponding to said frequency of said bus.

5. The method of claim 1, wherein fetching said data comprises:

fetching an initial amount of data from said memory component;

storing said initial amount of data in a storage device; and

fetching additional data from said memory component at least based on a threshold value of said storage device.

6. The method of claim 5, wherein fetching said data further comprises:

starting a timer; and

fetching additional data from said memory component when said timer has elapsed.

7. A mechanism to fetch data from a memory component, said mechanism comprising:

a control unit to receive an indication regarding a frequency of a bus; and

a storage device including a plurality of registers, each register to store parameters relating to data fetching based on a different frequency of said bus, said control unit to obtain said parameters based on said indication, said control device to further fetch said data from said memory component based on said parameters.

8. The mechanism of claim 7, wherein said parameters relate to a data transfer size.

9. The mechanism of claim 8, wherein said parameters further relate to a threshold value.

10. The mechanism of claim 7, wherein said control unit operates based on said parameters to:

fetch an initial amount of data from said memory component;

store said initial amount of data in said storage device; and

fetch an additional amount of data from said memory component at least based on a threshold value of said storage device.

11. The mechanism of claim 10, wherein said control unit further operates to:

start a timer; and

fetch a still further amount of data from said memory component when said timer has elapsed.

12. The mechanism of claim 7, wherein said control unit fetches a size of data from a memory subsystem on one side of a host chipset for a bus device on an opposite side of said host chipset as a function of said frequency of said bus.

13. The mechanism of claim 12, wherein said sizes of data are fetched from said memory subsystem on one side of said host chipset, via a primary bus, for the bus device on an opposite side of said host chipset, via a secondary bus.

14. The mechanism of claim 13, wherein said primary bus and said secondary bus correspond to Peripheral Component Interconnect (PCI) buses, and said host chipset corresponds to a PCI-PCI bridge of a computer system.

15. A computer system comprising:

a memory subsystem;

a host chipset to couple to said memory subsystem via a first bus; and

a bus device to couple to said host chipset via a second bus, wherein said host chipset fetches data from said memory subsystem for said bus device upon request, said host chipset comprising:

a buffer device to store data fetched from said memory subsystem via said first bus for said bus device;

a plurality of registers each to contain parameters corresponding to a different operating frequency of said second bus; and

a data fetching mechanism to receive an indication of an operating frequency of said second bus and to obtain said parameters corresponding to said operating frequency of said second bus based on said indication, said control device to fetch said data from said memory component based on said obtained parameters.

16. The computer system of claim 15, wherein said host chipset corresponds to a Peripheral Component Interconnect (PCI) 64-bit hub.

17. The computer system of claim 15, wherein said first bus and said second bus correspond to Peripheral Component Interconnect (PCI) buses, and said host chipset corresponds to a PCI-PCI bridge.

18. The computer system of claim 15, wherein said parameters correspond to: an initial request length, an initial threshold length, a subsequent request length, and a subsequent threshold length.

19. The computer system of claim 15, wherein said data fetching mechanism operates to:

fetch an initial amount of data from said memory subsystem;

store said initial amount of data in said buffer device; and

fetch an additional amount of data from said memory subsystem at least based on a threshold value of said buffer device.

20. The computer system of claim 19, wherein said data fetching mechanism further operates to:

start a timer; and

fetch a still further amount of data from said memory subsystem when said timer has elapsed.

21. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of fetching data from a memory component, said method comprising:

obtaining parameters relating to data fetching from said memory component based on an operating frequency of a bus; and

fetching said data from said memory component based on said obtained parameters.

22. The program storage device of claim 21, wherein fetching said data comprises:

fetching an initial amount of data from said memory component;

storing said initial amount of data in a storage device; and

fetching additional data from said memory component at least based on a threshold value of said storage device.

23. The program storage device of claim 22, wherein fetching said data further comprises:

starting a timer; and

fetching additional data from said memory component when said timer has elapsed.